GEC PLESSEY
SEMICONDUCTORS

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ADVANCE INFORMATION

DS3925 - 2.1

VP536A/VP536B*

NTSC/PAL DIGITAL VIDEO ENCODER

(supersedes DS3925 - 1.2, March 1994 & MS4013 - 1.0 July 1994)

FEATURES

- Converts RGB data (3x8bits) to analog composite video and S-video
- Internal video timing generation
- RGB or YUV input modes
- Progressive scanning (non-interlaced fields) display mode optional
- Separate horizontal and vertical sync outputs
- 68 pin PLCC package
- Better than 9 bit video accuracy

APPLICATIONS

- Multi-media
- Video Games
- PC's
- Graphics
- Display Adaptors
- Video Effects Processors

DESCRIPTION

The VP536A/VP536B converts digital RGB data (3x8bits) into analog NTSC/PAL (NTSC only for VP536A) composite video and S-video signals. The outputs are capable of driving doubly terminated 75 ohm loads with standard video levels.

The device will also accept gamma-corrected RGB data or YUV data. Progressive scan (non-interlaced fields) video display mode is available.

The output pixel rate is approximately 7 times Fsc (color subcarrier frequency) for NTSC (6.6 times Fsc for PAL) which is approximately 25MHz. Input pixel rate is half this frequency; approximately 12.5MHz.

All the necessary synchronization signals are generated internally. Digital horizontal and vertical sync outputs are available for use by the host system.

The rise and fall times of sync, burst envelope and video blanking are internally controlled to be within composite video specifications.

Two digital to analog converters (DACs) are used to convert the digital luminance and chrominance data into analog signals. An inverted composite video signal is generated by summing the complimentary current outputs of each DAC. An internally generated reference voltage provides the biasing for the DACs.

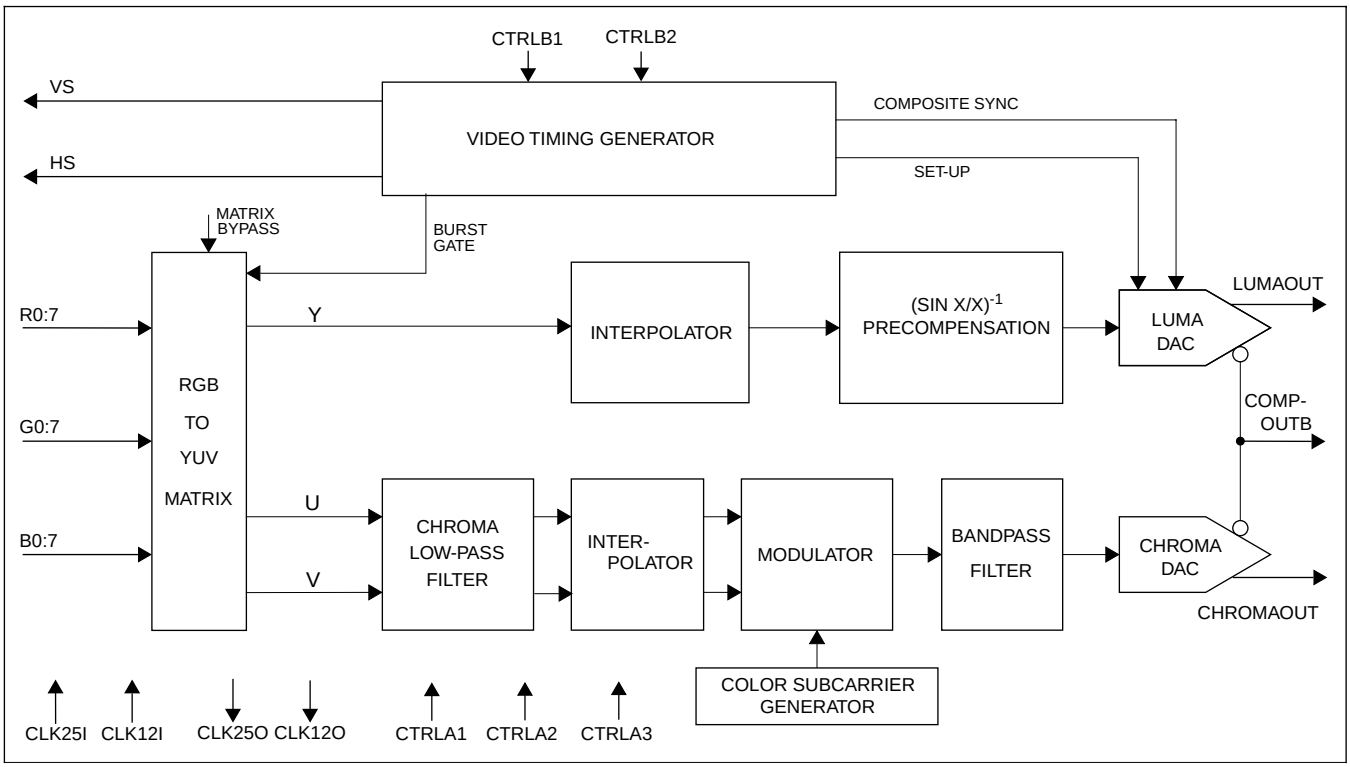


Fig. 1. Functional Block Diagram

* VP536A OPERATES IN NTSC ONLY.
VP536B OPERATES IN BOTH NTSC AND PAL MODES. VP536B IS A FUTURE DEVELOPMENT.

NTSC/PAL Video Standards

Both NTSC (4-field, 525 lines) and PAL (8-field, 625 lines) video standards are supported by the VP536B (NTSC only for VP536A). All raster synchronization, color subcarrier and burst characteristics are adapted to the standard selected. However, different input clock frequencies are necessary for each of the two video standards. For the NTSC mode of operation, input clock frequencies of 25.048948MHz. and 12.524474MHz. are required. For the PAL mode of operation on the VP536B, the required input clock frequencies are 29.500000MHz. and 14.750000MHz.

The mode of operation is selected through the CTRLB1 and CTRLB2 pins as shown in Table 1.

Progressive Scan Display

Progressive scanning (non-interlaced fields) display modes are available for both semi-NTSC and semi-PAL video applications. In both cases, field 1 is repeated while field 2 is discarded. An extra half line is included in field 1. Thus in the semi-NTSC mode, 263 lines of field 2 are retraced as field 1 resulting in 526 lines per frame, and similarly in the semi-PAL mode, 313 lines of field 2 are retraced as field 1 resulting in 626 lines per frame.

Progressive scanning display mode is selected through the CTRLB1 and CTRLB2 pins as shown in Table 1.

CTRLB2	CTRLB1	Video Standard
0	0	NTSC
0	1	Progressive Scan NTSC
1	0	PAL(VP536B only)
1	1	Progressive Scan PAL (VP536B only)

Table 1: VP536A/VP536B Modes of Operation

NOTE: CTRLB1 & CTRLB2 are internally pulled low, therefore, if left unconnected, NTSC is the default mode of operation.

Video Timing

The VP536A/VP536B has an internal sync generator which produces video timing signals appropriate to the mode of operation. All timing signals are derived from the two input clocks. These clocks are input on the CLK25I pin and the CLK12I pin. The two input clock frequencies for NTSC and PAL are related by a ratio of 2.

The lower frequency corresponds to the input pixel data rate. Input pixel data is latched in on the rising edge of the CLK12I clock.

The clocks must be derived from a crystal controlled oscillator in order to avoid timing, chroma frequency and modulation errors.

The video timing generator produces the internal composite sync, blanking and burst gate as well as externally available horizontal sync (HS) and vertical sync (VS) pulse signals. The HS and VS signals are negative true pulses coincident with the sync pulses in the output video signals.

The HS signal has the same duration as a standard horizontal sync pulse but is continuous through the vertical sync interval.

Input Pixel Data Format

Input pixel data may be in one of two formats; gamma corrected RGB and YUV. This format is controlled by the state of the pins CTRLA1, CTRLA2 and CTRLA3 according to the following table.

CTRLA2	CTRLA1	Input Pixel Data Format
0	0	reserved
0	1	RGB (gamma corrected)
1	0	YUV
1	1	reserved

Table 2: Input Pixel Data Format

NOTE: CTRLA1 is internally pulled high, while CTRLA2 & CTRLA3 are internally pulled low; therefore if left unconnected, gamma corrected RGB is the default input pixel data format. CTRLA3 is reserved.

The RGB input data coding is straight binary and is in the range of 0-255. In the YUV input mode, Y, U and V data is presented on the R, B and G input data buses, respectively. Y data coding is binary and is in the range of 0-247. U and V coding is in two's complement binary. U is in the range of -102 to +102 and V is in the range of -107 to +107.

Video Blanking

The VP536A/VP536B automatically performs standard composite video blanking. Lines 1-17, 261-279, 523-525 inclusive, as well as the last half of line 260 and the first half of line 280 are blanked in the NTSC mode. In PAL mode on the VP536B, lines 1-22, 311-335, 624-625 inclusive, as well as the last half of line 623 and the first half of line 23 are blanked.

The host pixel data can be phased relative to the active video timing by counting the CLK12I clock periods from the rising edge of HS. NTSC active video starts 48 CLK12I clock cycles after the rising edge of the horizontal sync pulse output, and PAL active video starts 58 CLK12I clock periods after the rising edge of HS (HS and VS pulse edges coincide with the rising edge of the CLK12I clock).

Input pixel data is ignored during the composite blanking periods.

Color Space Matrix

The RGB color space is converted to a YUV color space, using a transformation matrix defined by the NTSC and PAL colorimetry definitions. If the input data format is YUV, this block is bypassed without affecting the overall data latency.

Interpolator

The luminance and chrominance data is separately passed through interpolating filters to produce output sampling rates double that of the incoming pixel rate. This reduces the sinx/x distortion that is inherent in the digital to analog converters and also simplifies the analog reconstruction filter requirements.

Sinx/x Distortion Precompensation

The luminance data is precompensated for the sinx/x distortion that is inherent in the digital to analog converters. Since the chrominance data is contained within a relatively narrow frequency range, it's sinx/x distortion is compensated for by increasing the gain of the chrominance DAC by a fixed amount.

Digital To Analog Converters

The VP536A/VP536B contains two 8-bit digital to analog converters which produce the analog video signals. The DACs use a current steering architecture in which bit currents are routed to one of two outputs; thus each DAC has a true and complimentary output. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed. An on-chip voltage reference of 1.0V (typ.) provides the necessary biasing. However, the VP536A/VP536B may be used in applications where an external 1V reference is provided, to adjust the video levels. In this case the external reference should be temperature compensated and provide a low impedance output.

The full-scale output currents of the DACs is set by external resistors between the LUMAGAIN, CHROMAGAIN and GND pins. An on-chip loop amplifier stabilizes the full-scale output current against temperature and power supply variations.

By summing the complimentary current outputs of the two DACs, an inverted composite video signal is obtained. Note that this signal has a DC offset. The analog outputs of the VP536A/VP536B are capable of directly driving a 37.5 ohm load, such as a doubly terminated 75 ohm co-axial cable.

DAC Gain Adjust

The gains of the luma and chroma DACs are independently adjustable. The gains are adjusted using the external gain setting resistors between the LUMAGAIN, CHROMAGAIN pins and GND.

For the correct DAC gains in the NTSC mode, the LUMAGAIN resistance should be 905ohms. The CHROMAGAIN resistance should be 562ohms for the proper corresponding chroma amplitude (including sinx/x compensation).

For the correct DAC gains in the PAL mode on VP536B, the LUMAGAIN resistance should be 837ohms and the CHROMAGAIN resistance should be 520ohms for the proper corresponding chroma amplitude (including sinx/x compensation).

Luminance, Chrominance & Composite Video Outputs

The Luminance video output (LUMAOUT pin) drives a 37.5 ohm load at 1.0V, sync tip to peak white. It contains only the image's luminance content plus the composite synchronization pulses. In the NTSC mode, a Set-Up Level offset is added during the active video portion of the raster.

The chrominance video output (CHROMAOUT pin) drives a 37.5 ohm load at levels proportional in amplitude to the luma output (40 IRE pk-pk burst). This output has a fixed offset current which will produce approximately a 0.5V DC bias across the 37.5 ohm load. Burst is injected with appropriate timing relative to the luma signal.

Luma, Chroma and true Composite video signals may be obtained simultaneously through the use of an external inverting video amplifier with the inverted composite video output (COMPOUTB pin).

The inverted composite video output has a fixed DC offset. Sync tip is the most positive voltage and is approximately 1.5V with a 37.5 ohm load.

The NTSC output video waveforms of the luma, chroma and inverted composite signals for 100% amplitude, 100% saturated color bars are shown in Figs. 3-5.

Extendable S-Video Bandwidth

The bandwidth of color baseband signals is typically limited in order to avoid modulation problems that develop in composite video as the bandwidth approaches that of the subcarrier frequency. The VP536A/VP536B can use either traditional bandwidth limited or extended bandwidth baseband signals. For applications where the composite signal is the main source of the video display, it is recommended that bandwidth limiting be used in order to avoid "dot-crawl" effects in the display. For S-Video applications where the luma and chroma signals are separate, enabling the extended bandwidth will result in improved picture definition.

The enabling/disabling of this bandwidth extension is controlled through the TCSPK pin as shown below.

TCSPK	Chroma Bandwidth
0	Extended Bandwidth
1	Limited Bandwidth

Table 3: Bandwidth Control

NOTE: TCSPK is internally pulled LOW, therefore Extended Bandwidth is the default selection.

Master Reset

The VP536A/VP536B can be initialized with the RESET pin. This is an active low signal and must be active for a minimum of 2 CLK12I clock periods in order for the VP536A/VP536B to be reset. The device resets to line 64, start of horizontal sync (ie line blanking active). There is no on-chip power on reset circuitry.

Video Timing Reset

The VP536A/VP536B also features the ability to independently reset the video timing generator without affecting the data path. The TSURST pin controls this function. Taking this pin high resets the video timing generator. If this pin is left open, it is internally pulled low. This feature can be usefull here two independent video sources are used.

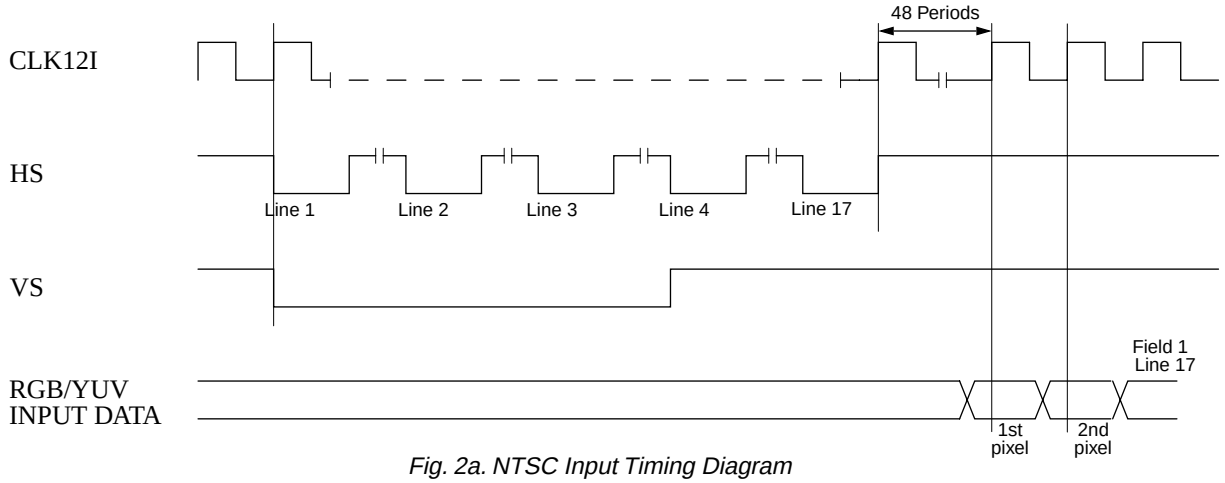


Fig. 2a. NTSC Input Timing Diagram

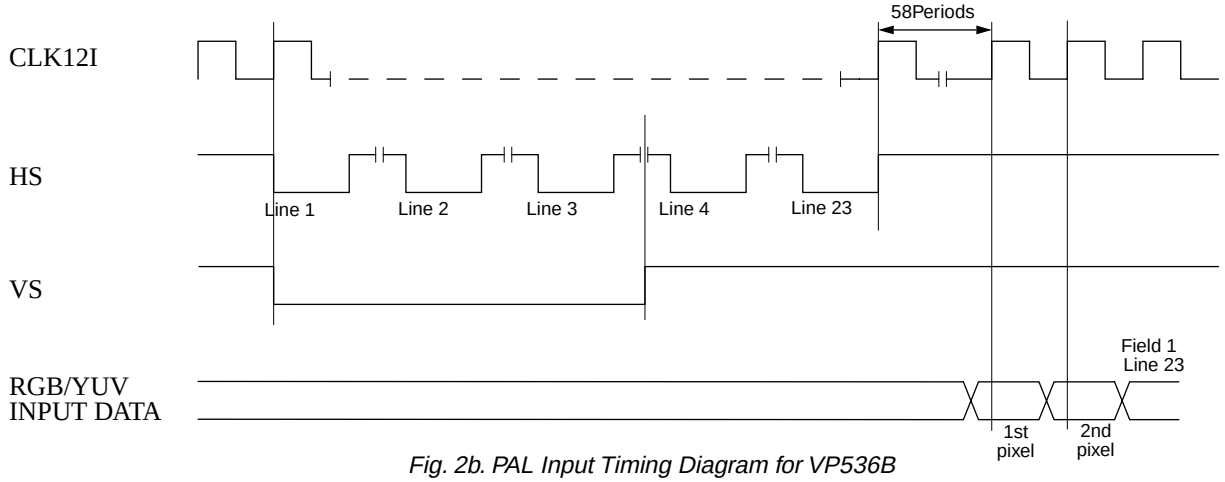


Fig. 2b. PAL Input Timing Diagram for VP536B

NOTE:

1. Coincident falling edges of HS and VS denote the start of an odd field.
2. VS is low during the first 3 lines in each NTSC field and during the first $2^1/_2$ lines in each PAL field.
3. Input pixel data is ignored during composite blanking periods.

Fig. 3.
NTSC Luminance Video Output Waveform

100% saturation, 100% amplitude color bars.

LUMAGAIN resistor = 905 ohms, VREF=1.0V, 37.5ohm load. typical current values

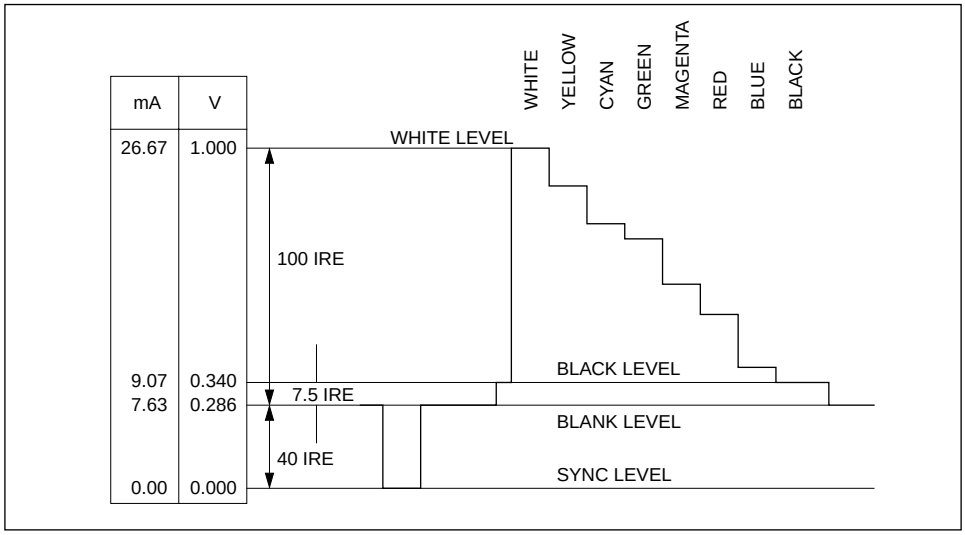


Fig. 4.
NTSC Chrominance Video Output Waveform

100% saturation, 100% amplitude color bars.

CHROMAGAIN resistor = 562ohms, VREF=1.0V, 37.5ohm load. typical current values

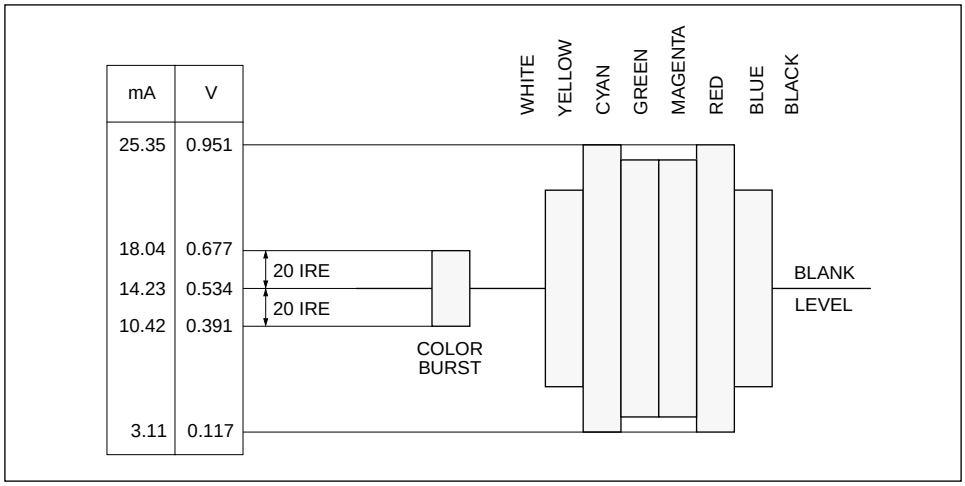
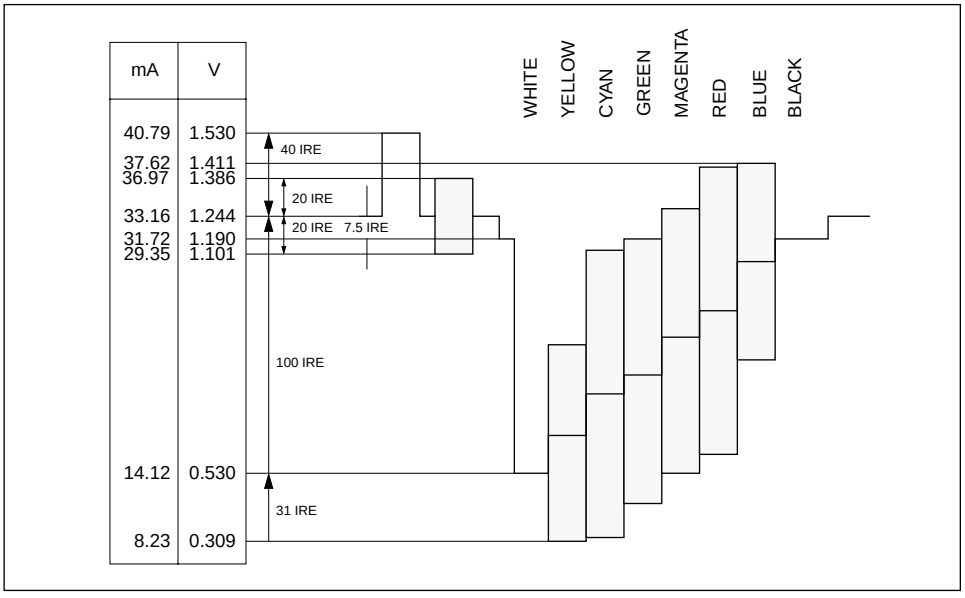


Fig. 5.
NTSC Inverted Composite Video Output Waveform

100% saturation, 100% amplitude color bars.

LUMAGAIN resistor = 905 ohms, CHROMAGAIN resistor = 562ohms, VREF=1.0V, 37.5ohm load typical current values



Pin Descriptions

Pin Name	Pin No.	Description
B0-B7	2-9	8 Bit Blue data inputs. B0 is the least significant bit, corresponding to Pin 2. These pins are internally pulled low.
G0-G7	17-24	8 Bit Green data inputs. G0 is the least significant bit. These pins are internally pulled low. G0 is pin 17
R0-R7	62-68, 1	8 Bit Red data inputs. R7 is the most significant bit corresponding to Pin 1. These pins are internally pulled low.
CLK25I	57	2X pixel rate clock input. The VP536A/VP536B requires a clock whose frequency is twice the input pixel data rate; i.e., 25.0489484MHz. for the NTSC mode of operation, and with the VP536B, 29.500000MHz. for the PAL mode of operation.This clock must be derived from a crystal controlled oscillator in order to avoid chroma frequency, modulation and timing errors.
CLK12I	60	Pixel rate clock input. The frequency of this clock must be exactly half that of the CLK25I clock.
CLK25O	61	2X pixel rate clock output. The CLK25I clock is output on this pin. Note that this output clock signal is inverted with respect to the CLK25I clock.
CLK12O	51	Pixel rate clock output. The CLK12I clock is output on this pin.
HS	14	Horizontal sync pulse output. This is an active low signal output, i.e. the presence of a sync pulse is denoted by the signal being low.
VS	13	Vertical sync pulse output. This is an active low signal output.
RESET	16	VP536A/VP536B master reset. This is an active low input signal and must be asserted for a minimum of 2 CLK12I clock periods in order to reset the VP536A/VP536B.
CTRLA1 CTRLA2 CTRLA3	59 58 54	Input data format control. Control codes on these three input pins determine the format of the input data as described in Input Pixel Data Format on Page 2. CTRLA1 is internally pulled high, while CTRLA2 and CTRLA3 are internally pulled low; therefore if left open, the default input data format is gamma corrected RGB.
CTRLB1 CTRLB2	52 53	Video standard control. Control codes on these two input pins determine the video display mode as described in Table 2 on Page 2. These pins are internally pulled low, therefore if left open, the default video display mode is NTSC.
TCSPK	49	Enable/Disable extended video bandwidth. Taking this pin high limits the bandwidth of the video signal as described in Extendable S-Video Bandwidth on Page 3. This pin is internally pulled low, therefore if left open, extended bandwidth is enabled.
TSURST	50	Synchronous reset of video timing. An active high pulse on this pin resets the video timing generator without affecting the data path. On the rising edge of CLK12I following TSURST going low, Field 1, line 1 is initiated. This pin is internally pulled low.
VREF	28	Voltage reference output. This output is nominally 1.0V and should be decoupled with a 0.1uF capacitor to GND.
LUMA-COMP	30	Luma DAC compensation. A 0.1uF ceramic capacitor must be connected between pin 30 and pin 31.
CHROMA-COMP	38	Chroma DAC compensation. A 0.1uF ceramic capacitor must be connected between pin 38 and pin 37.
LUMAOUT COMPOUTB CHROMAOUT	32 34 36	Luminance, inverted composite and chrominance video signal outputs. These outputs are high impedance current source outputs. A DC path to GND must exist from each of these pins.
LUMAGAIN	29	Luminance full scale current control. A resistor connected between this pin and GND sets the magnitude of the luminance video output current. An internal loop amplifier controls a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage. This reference current has a weighting equal to 16 LSB's. Note that the IRE relationships shown in Fig. 3 are maintained, regardless of the output full scale current.

Table 4: Pin Descriptions

Pin Name	Pin No.	Description
CHROMAGAIN	39	Chrominance full scale current control. As with the LUMAGAIN pin, a resistor between this pin and GND controls the magnitude of the chrominance video signal. An internal loop amplifier adjusts a reference current flowing through this resistor so that the voltage across it is equal to the Vref voltage. This reference current has a weighting equal to 16 LSB's.
TEST0-TEST7	41-48	These pins must be tied low.
CTRLC1 CTRLC2	15 12	Test mode control. These two pins are used to configure the VP536A/VP536B into various test modes. They should be held low during normal operation.
VAA	10, 25, 31, 37, 40, 55	Positive supply input. All VAA pins must be connected.
GND	11, 26, 56 27, 33, 35	Negative supply input (GND). All GND pins must be connected.

Table 4: Pin Descriptions (Continued)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	VAA	4.75	5.00	5.25	V
Power supply current	IAA		200		mA
Input clock frequency					
CLK25I (NTSC)			25.048948		MHz.
CLK12I (NTSC)			12.524474		MHz.
CLK25I (PAL - VP536B)			29.500000		MHz.
CLK12I (PAL - VP536B)			14.750000		MHz.
CLK25I & CLK12I rising edges must be synchronous					
Input clock frequency accuracy				25	ppm
Analog video output load			37.5		Ω
Gain resistors					
Lumagain resistor (NTSC)			905		Ω
Chromagain resistor (NTSC)			562		Ω
Lumagain resistor (PAL - VP536B)			837		Ω
Chromagain resistor (PAL - VP536B)			520		Ω
Ambient operating temperature		0		70	^{o}C

ABSOLUTE MAXIMUM RATINGS (Referenced to GND)

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply	VAA	-0.3		7	V
Voltage on any non-power pin		-0.3		VAA + 0.3	V
Analog video output short circuit duration			Indefinite		
Ambient operating temperature		0		70	^{o}C
Storage temperature		-55		125	^{o}C

NOTE: Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions

DC Characteristics (see note on Page 11)

Parameter	Symbol	Min.	Typ.	Max.	Units
Resolution (each DAC)		8			Bits
Accuracy (each DAC)					
Integral linearity error	INL			+/- 1.5	LSB
Differential linearity error	DNL			+/- 1	LSB
Gray scale error				+/- 5	% gray scale
Monotonicity			Guaranteed		
Analog video output compliance	V_{AVOC}	-0.3		1.6	V
Digital Inputs					
Input high voltage	V_{IH}	3.0			V
Input low voltage	V_{IL}			0.8	V
Digital Outputs					
Output high voltage (I_{OH} = -10.0 mA)	V_{OH}	VAA - 1			V
Output low voltage (I_{OL} = 10.0 mA)	V_{OL}			0.4	V
Luminance video output current					
White level relative to black level (NTSC)		16.74	17.6	18.46	mA
			255		LSB
Black level relative to blank level (NTSC)		0.95	1.44	1.90	mA
			21		LSB
Blank level relative to sync level (NTSC)		6.30	7.63	8.96	mA
			111		LSB
LSB size (NTSC)			69.1		µA
White level relative to black/blank level (PAL -VP536B)			tbd		
Black/blank level relative to sync level (PAL -VP536B)			tbd		
LSB size (PAL -VP536B)			tbd		
Chrominance video output current					
Blank level (NTSC)		13.51	14.23	14.95	mA
Peak chroma level relative to blank level (NTSC) (corresponding to 100% saturated red)		+/- 10.12	+/- 11.12	+/- 12.12	mA
Peak burst level relative to blank level (NTSC)		+/- 3.46	+/- 3.81	+/- 4.16	mA
LSB size (NTSC)			111.2		µA
Blank level (PAL -VP536B)			tbd		
Peak chroma level relative to blank level (PAL) (corresponding to 100% saturated red) (-VP536B)			tbd		
Peak burst level relative to blank level (PAL -VP536B)			tbd		
LSB size (PAL -VP536B)			tbd		
Internal reference voltage	V_{REF}	0.95	1.00	1.05	V
Internal reference voltage output impedance			tbd		KΩ

AC Characteristics (see note on Page 11) Rise and fall times are measured between 10% and 90% of the final values

Parameter	Symbol	Min.	Typ.	Max.	Units
CLK12I clock delay with respect to CLK25I clock	t_{dCLK}	2		18	ns Note 1
Data set-up time (wrt CLK12I clock)	t_{suDATA}	8			ns
Data hold time (wrt CLK12I clock)	t_{hDATA}	5			ns
HS/VS output delay wrt CLK12I clock	t_{dSYNC}	0		20	ns
HS low pulse width (NTSC)	$t_{wHS\text{-}NTSC}$		59		CLK12I cycles
HS low pulse width (PAL -VP536B)	$t_{wHS\text{-}PAL}$		tbd		CLK12I cycles
VS low pulse width(NTSC)	$t_{wVS\text{-}NTSC}$		2388		CLK12I cycles
VS low pulse width (PAL -VP536B)	$t_{wVS\text{-}PAL}$		tbd		CLK12I cycles
Input clock pulse width high time		16			ns
Input clock pulse width low time		16			ns
Analog video output delay (wrt CLK25I clock)	t_{dAVO}		10		ns
Analog video output rise/fall time	t_{rfAVO}		8		ns
Analog video output settling time (50% to +/- 1 LSB)	t_{sAVO}		12		ns
Glitch impulse			100		pV-sec
Signal related harmonics of DAC outputs for 1MHz. direct digitally synthesized sine wave			tbd		dB
Pipeline delay (data in to analog video out)			tbd		
Power supply rejection ratio (chromacomp, lumacomp = 0.1uF, f = 1 KHz.)			40		dB

Note 1 Tests are taken at 50% duty cycle on CLK12I and CLK25I.

Timing Waveforms

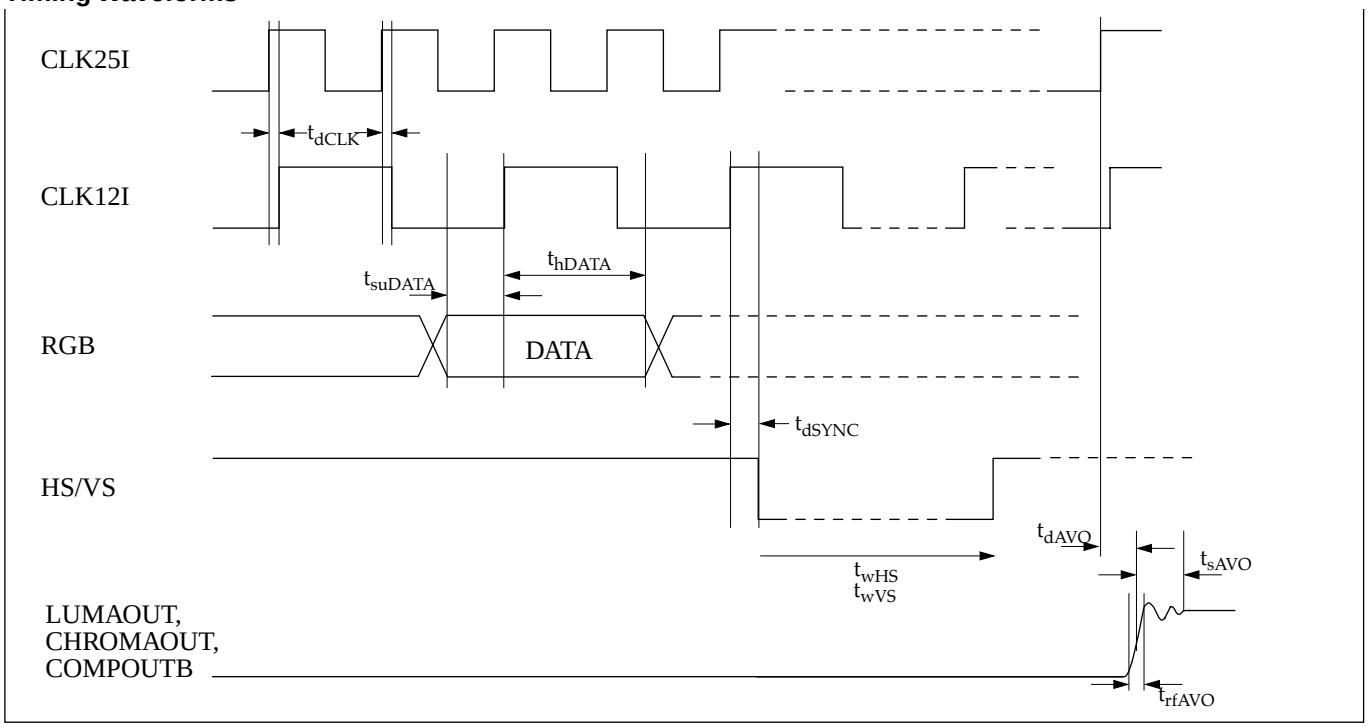


Fig. 6. Input/Output Timing Diagram

Video Characteristics (see note below) Rise and fall times are measured between 10% and 90% of the final values

Parameter	Symbol	Min.	Typ.	Max.	Units
Luminance bandwidth (Extended Bw mode)			4.0		MHz.
Luminance bandwidth (Reduced Bw mode)			2.5		MHz.
Chrominance bandwidth (Extended Bw mode)			1.8		MHz.
Chrominance bandwidth (Reduced Bw mode)			1.2		MHz.
Burst frequency (NTSC)			3.579545		MHz.
Burst frequency (PAL -VP536B)			4.433619		MHz.
Burst cycles (NTSC)			10		Fsc cycles
Burst cycles (PAL -VP536B)			10		Fsc cycles
Burst envelope rise/fall time			1.5		Fsc cycles
Analog video sync rise/fall time			90		ns
Analog video blank rise/fall time			160		ns
Differential gain			1.5		% pk-pk
Differential phase			1.0		^{o} pk-pk
Signal to Noise Ratio (white field)			60		dB
Chroma AM signal to noise ratio (100% red field)			58		dB
Chroma PM signal to noise ratio (100% red field)			56		dB
Hue accuracy				2.5	%
Color saturation accuracy				2.5	%
Residual subcarrier			-60		dB
Luminance/chrominance delay			20		ns

NOTE: The DC, AC and Video characteristics listed above are based on design targets and/or actual measurements on a limited number of devices. All parametric information is subject to review following further characterization.

Pin No.	Pin Name	Pin No.	Pin Name
1	R7	35	GND
2	B0	36	CHROMAOUT
3	B1	37	VAA
4	B2	38	CHROMACOMP
5	B3	39	CHROMAGAIN
6	B4	40	VAA
7	B5	41	TEST0
8	B6	42	TEST1
9	B7	43	TEST2
10	VAA	44	TEST3
11	GND	45	TEST4
12	CTRLC2	46	TEST5
13	VS	47	TEST6
14	HS	48	TEST7
15	CTRLC1	49	TCSPK
16	RESET	50	TSURST
17	G0	51	CLK12O
18	G1	52	CTRLB1
19	G2	53	CTRLB2
20	G3	54	CTRLA3
21	G4	55	VAA
22	G5	56	GND
23	G6	57	CLK25I
24	G7	58	CTRLA2
25	VAA	59	CTRLA1
26	GND	60	CLK12I
27	GND	61	CLK25O
28	VREF	62	R0
29	LUMAGAIN	63	R1
30	LUMACOMP	64	R2
31	VAA	65	R3
32	LUMAOUT	66	R4
33	GND	67	R5
34	COMPOUTB	68	R6

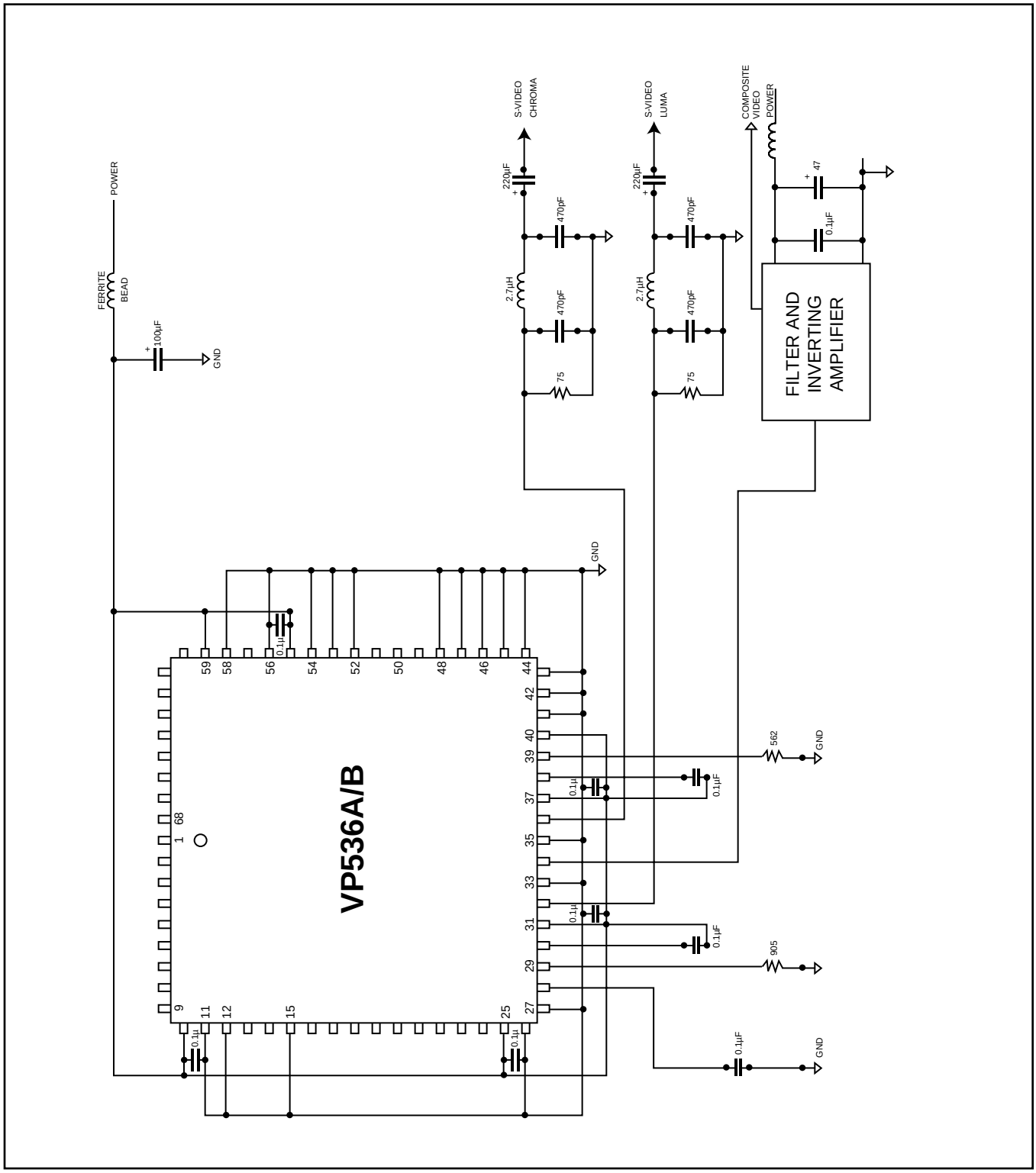


Fig. 7. Recommended external component connections for NTSC

VP536A/VP536B PCB LAYOUT RECOMMENDATIONS

To obtain the optimum performance from the VP536A/VP536B video encoder, care must be taken in the PCB layout to ensure low noise power and ground lines. This can be achieved by using power and ground planes, shielding the digital inputs and providing good decoupling.

Power and Ground Planes

Ideally, the VP536A/VP536B and its associated circuits should have its own separate power and ground planes, which should be connected at a single point through a ferrite bead (such as Ferroxcude 5659065-3B, TDKBF45-4001 or Fair-Rite 2743001111) to the regular PCB power and ground. However, a separate analog power plane with a connection through a ferrite bead, along with a common ground plane should be used as a minimum. It is important that the regular PCB power and ground planes do not overlay portions of the analog power or ground planes to minimize plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane will be further reduced by the use of multiple decoupling capacitor. Optimum performance is obtained with 0.1μF chip ceramic capacitors placed as close as possible to the VAA pins, with the shortest leads possible to reduce lead inductance. Connecting a similar 0.1μF capacitor between the LUMACOMP/CHROMACOMP and its neighboring VAA pins will help to improve high frequency power supply rejection.

Digital Signal Interconnect

The digital signal lines to the VP536A/VP536B should be isolated as much as possible from the analog circuitry. Due to the high clock rates used, the clock lines to the VP536A/VP536B should be as short as possible to minimize noise pickup.

Analog Signal Interconnect

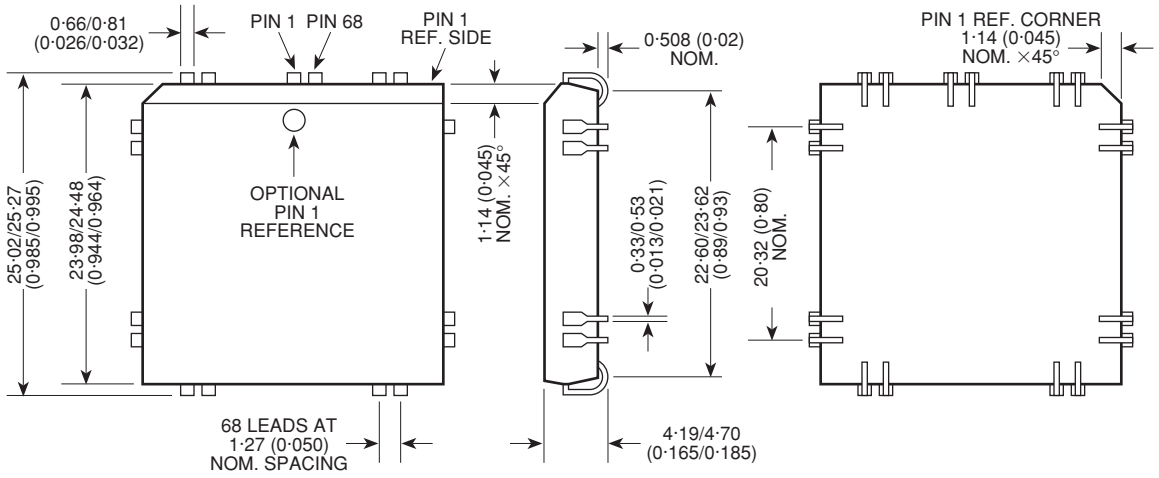
For optimum performance, the analog video output filters as well as the composite video inverting circuit should be located as close as possible to the VP536A/VP536B to minimize noise pickup. The video output signals should overlay the ground plane and not the analog power plane, to maximize the high frequency power supply rejection.

Ordering Information

NTSC Only version: VP536A/CG/HPAS
NTSC and PAL version: Contact your local sales office for availability.

Package Details and Pin-Out

All dimensions shown in mm/(inches)



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

68-LEAD QUAD PLASTIC J-LEAD – HP68

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